



(\*) This piece of NAND gates is pulling down the D6 bit of data bus, when any read operation is done at \$D500-\$D5FF area.

Software protected by this circuit, reads periodically or in random way the \$D5xx area, then checks that bit D6 is always set to zero, when logic "1" occurs that means that protection circuit doesn't exist.

Title		
Blizzard Excelent Cartridge (pirated version by Polish Cracking Crew)		
Size	Number	Revision
A4	(rev. eng. from real hardware)	1.0
Date:	2019-01-19	Sheet 1 of 1
File:	F:\[projects]\_blizzard excelent.SchDoc	Drawn By: Seban / Slight